Abstracts

Numerical Simulation of GaAs MESFET's with a p-Buffer Layer on the Semi-Insulating Substrate Compensated by Deep Traps

K. Horio, Y. Fuseya, H. Kusuki and H. Yanai. "Numerical Simulation of GaAs MESFET's with a p-Buffer Layer on the Semi-Insulating Substrate Compensated by Deep Traps." 1989 Transactions on Microwave Theory and Techniques 37.9 (Sep. 1989 [T-MTT] (Special Issue on FET Structures Modeling and Circuit Applications)): 1371-1379.

Numerical simulation of GaAs MESFET's with a p-buffer layer on the semi-insulating substrate is performed in which impurity compensation by traps in the substrate is considered. It is shown that the use of a thicker p-buffer layer results in lower device current due to the formation of a steeper barrier at the channel-substrate interface. It is also shown that in a case with higher acceptor and trap densities in the substrate, the drain current becomes lower due to the decrease in the substrate current. This decrease in the substrate current occurs due to the formation of a negative space-charge layer in the substrate. It is concluded that using a thick p-buffer layer has the same effect as using a substrate with a high density of traps inasmuch as both of them lead to minimizing the short-channel effects in GaAs MESFET's.

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